REMARKS

Claims 1, 9, 31, 53, 57, have been amended. Claims 2-4, 10-14, 20, 32-36, 61-65, and 71-72 have been canceled. Claims 1, 7-9, 15-19, 21-28, 30-31, 37-50, 52-53, 57-60, 66-70, 73-75, and 77 are pending.

Claims 1-4, 7-30, 57-75, and 77 stand rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the written description requirement. The Office Action has alleged that there is no support for disposing the "receiver/driver pairs," the "device," and "other elements" on an integrated circuit. These limitations have been removed from the claims, as they are not required for patentability. Accordingly, the rejection under 35 U.S.C. § 112, first paragraph, should be withdrawn.

Nevertheless, it should be noted that these former limitations are, in fact, supported by the application. More specifically, the Examiner's attention is respectfully directed to claim 5 of the as-filed application (now canceled), which recited "where said first and second receiver and driver pairs are located on a same integrated circuit as a memory device." The Examiner's attention is further directed Fig. 15 and the corresponding description on page 9 of the application, specifically:

> It should be understood that connection to a conversion circuit 45 is not required, and instead, the first and second receiver and driver pairs 212, 214 may be connected directly to an I/O device (e.g., a memory device), as illustrated in FIG. 15. Thus, the first and second receiver and driver pairs 212,214 may be integrated into other system components and may be located, for example, on a memory device (e.g., 54), or on a memory module (e.g., 24).

The specification therefore provides ample support for disposing the recited device upon an single integrated circuit.

Claim 31-37, 40, 43-45, 48-49, and 52-53 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Leddigie (U.S. Patent No. 6,587,912). Claims 1-4, 7-15, 18, 21-23, 26-27, 30, 57-65, 73-75, and 77 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Leddige in view of Puar (U.S. Patent No. 5,703,806). Claims 28 and 50 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Leddige in view of Official Notice. Claims 16-17, 19-20, 24-25, 38-39, 41-42, 46-47, 66-67, and 69-72 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Leddige in view of Halbert (U.S. Patent No. 6,625,687). These rejections are respectfully traversed.

Claim 1 recites, *inter alia,* "a selector circuit connected to said first and second receiver and driver pairs, said selector circuit selectively operating said first and second receiver and driver pairs according to a state of a command/address bus coupled to said selector circuit such that in a first state of said command/address bus said first receiver and driver pair passes data between said first bus segment and an I/O device and bypasses said second bus segment, and in a second state of said command/address bus said first and second receiver and driver pairs pass data between respective adjacent bus segments and bypass said I/O device" and "wherein said first and second segments of said first bus is of a first data width and said I/O device is of a second data width, said first and second data widths being unequal."

Claim 9 recites, *inter alia,* "an interface circuit coupled to a command/address bus, said first and second receiver and driver pairs, and said second data bus; wherein said interface circuit is configured, based on a state of said command/address bus, to receive data from said first receiver and selectively place said data for said device on said second data bus and receive data on said second data bus and selectively place said data on said first data bus, and said first and second segments of said first data bus is of a first data width and said second data bus is of a second data width, said first and second data widths being unequal."

Claim 31 recites, *inter alia,* "an interface circuit coupled to a command/address bus, said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured, based on a state of said command/address bus, to receive data from said first receiver and selectively place said data for the memory on said second data bus, and receive data from the memory on said second data bus and selectively place said data on said first data bus" and "wherein said first and second segments of said first data bus is of a first data width and said second data bus is of a second data width, said first and second data widths being unequal; and said second bus is coupled to said memory."

Claim 53 recites, *inter alia,* "an interface circuit coupled to a command/address bus, said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured, based on a state of said command/address bus, to receive data for the device on said first data bus and selectively place said data on said second data bus, and receive data from the device on said second data bus and selectively place said data on said first data bus; wherein said first data bus is of a first data width, said second data bus is of a second data width, said first and second data widths being unequal."

Claim 57 recites, *inter alia,* "driving data using first and second drivers coupled to said respective first and second segments, said driving being performed according to a state of a command/address bus such that when said command/address bus is in a first state a first receiver and driver pair passes signals between said first segment of said first data bus and an I/O device and bypass said second segment, and when said command/address bus is in a second state said first and a second receiver and driver pairs pass signals between respective adjacent bus segments and bypass said I/O device" and wherein said first data bus is of a first data width, said I/O device is of a second data width, said first and second data widths being unequal."

Claim 60 recites, *inter alia,* "based on a state of an command/address bus coupled to said interface circuit, selectively placing data received from said first bus segment on said second bus segment when said command/address bus is in a first state; selectively placing data received from said second bus segment on said first bus segment when said command/address bus is in a second state; and selectively converting data received from one of said first and second data buses for use on the other of said first and second data buses; wherein said first data bus is of a first data width, said second data bus is of a second data width, said first and second data widths being different."

Referring to Figs. 3-5, Leddgie discloses a computer memory system which includes plural segments of a first bus 300 ad a second bus 321. When the repeater hub receives bus traffic on the first bus targeted for a memory device 301 on the second bus associated with the hub, the hub routes that signal from the first bus to the second bus. Otherwise, the hub routes that signal further along (i.e., from the first segment to the second segment) the first bus 300. In this manner, more memory devices than the limitation imposed by having only a first bus can be associated with the memory system. Column 4, lines 6-9.

Significantly, in Leddgie, the first and second buses are generally serial buses (Figs. 3-5), although in one alternative embodiment (see Fig. 7), the first bus is a parallel bus which carries commands, addresses, data, and optionally, one or more clock signals.

Leddgie, therefore fails to disclose or suggest the above quoted portions of the independent claims, each of which require a memory hub to selectively route data among two data buses of differing widths.

The Office Action additionally takes Official Notice that RF signals are known to be used for data communications, and further cites to Puar, which discloses a graphics controller, and Halbert, which discloses a memory module. However, neither the Official Notice, nor the disclosures of Paur and Halbert, whether taken individually, or in combination with each other and/or Leddgie, disclose or suggest a memory system having the features of the above quoted independent claims.

Accordingly, independent claims 1, 9, 31, 53, 57, and 60 are believed to be allowable over the prior art of record. Depending claims 7-8, 15-19, 21-28, 30, 37-50, 52, 58-59, 66-70, 73-75, and 77 are also believed to be allowable, for at least the same reasons as their respective independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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